UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/943,209	08/29/2001	William K. Lam	0007056-0186/P5729/KO	8850

32615 7590 03/11/2005		EXAMINER	
OSHA & MAY L.L.P./SUN		VU, TUAN A	
1221 MCKINNEY, SUITE 2800		ART UNIT	PAPER NUMBER
HOUSTON, TX 77010		2124	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	Application No.	Applicant(s)
	09/943,209	LAM ET AL.
	Examiner	Art Unit	
	Tuan A Vu	2124	

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _15 November 2004_.
2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-8_ is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) _1-8_ is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All   b)☐ Some * c)☐ None of:
        1.☐ Certified copies of the priority documents have been received.
        2.☐ Certified copies of the priority documents have been received in Application No. _____.
        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.   This action is responsive to the Applicant's response filed 11/15/2004.

As indicated in Applicant's response, no claims have been amended. Claims 1-8 are

pending in the office action.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Darty, USPN:

6,173,440 (hereinafter Darty), in view of Porterfield, USPN: 6,513,154 (hereinafter Porterfield).

As per claim 1, Darty discloses a method of debugging software comprising:

obtaining a software target file (e.g. *S102* – Fig. 3a);

obtaining a first input test vector (e.g. *S104*– Fig. 3a);

generating a first output vector (e.g. *S129* – Fig. 3b) by applying said first input test

vector to said target file;

applying a comparison test to said first output vector to determine whether a bug exists in

said module (*S137* – Fig. 3C); and

applying a module decomposition test to said module when the result of the comparison

is positive (e.g. *S139-S150, S160* – Fig. 3c-d – Note: branching back to step S102 reads on

decomposing yielding positively isolated set of module block codes upon which the testing cycle

is to be iteratively repeated);

But Darty does not explicitly disclose obtaining a bug list and appending said software module and said first input test vector to said bug list when the decomposition test result is negative. However, Darty creates matrix for mapping block of code to test points in relation with the input and output analysis based on block dependencies (Fig. 5; col. 16, lines 41-47; col. 17, line 28-40); and isolating of blocks of code iteratively in order to achieve a point where there is no subset of code with a failure (S153 – Fig 3d), disclosing that the blocks of code still with failure is being separated into further subblocks until the failure is detected. Appending the test being performed to test a block of code to a representation of such block was a known concept in test case at the time the invention was made, i.e. Darty from above has suggested creating a test list (*Test point mapping matrix* – col. 13, lines 47-55; col. 17, line 28-40) wherein each entry is composed of a code section and the corresponding test being performed on it; or its test designation or the input being used to activate the test like input vector. Creating such a code and test/input mapping is taught by the bug list by Porterfield (e.g. steps 34-39, Fig. 5). It would have been obvious for one of ordinary skill in the art at the time the invention was made to create the mapping matrix so that it lists a mapping of code and input vector as suggested above and taught by Porterfield because this would put forth a visual set of evidence from the test process which would instruct on the correspondence between the specific subdivision of the software being tested and the input or task being used to correlate such subdivision with isolating a bug location, enabling long term software development activities notwithstanding the changes in software as mentioned by Portefield (see col. 2 line 20 to col. 4, line 47).

As per claim 2, Darty discloses obtaining a predetermined output result vector and comparing first output vector to said predetermined output vector and determine whether said

first output is at variance with said predetermined output result vector (e.g. S131 – Fig. 3b –

Note: the fact of comparing inherently teaches whether or not actual output deviates or how far it

does from a standard median of the expected result, i.e. whether within acceptable variance

margin); but does not explicitly disclose an optimal output result vector. Official notice is taken

that the establishing of predicted or reference outputs being based on result from iterating from a

plurality of tests being applied on a target object in order to obtain the least deviated and

significant figures for legacy referencing, i.e. optimal results, was a known concept in the art of

software testing at the time the invention was made. Thus, it would have been obvious for one of

ordinary skill in the art at the time the invention was made to implement the storing of reference

output vectors as taught by Darty (S120 – Fig. 3b) so that such recorded output vector is a result

optimized or averaged out value, i.e. optimal output vector, obtained from previous test output

values being tallied on a specific target module, because persisting of the optimal value garnered

from a plurality of test values would enable the most averaged out value to represent the output

vector pertaining to different instances of test vectors or cases; thereby averting possible wide

divergence in output values that would not fit to for persistence and/or further referencing.

As per claim 3, Darty does not explicitly disclose obtaining a module decomposition list

comprsing 2 or more submodules when the result of said decomposition test is positive; and

iteratively processing said decomposition list. But in view of the pushing of the decomposition

as suggested by the combination of Darty (combined with Porterfield) from above, these

limitations would fall under the same ambit as segregating blocks of code that still have

failure(s) and repeat the test/comparing process (Fig. 3c-d – Note: decomposed blocks with 2 or

more sub-modules is disclosed in that the decomposition would have stopped if there is no faulty

sub-block to analyze) and such teaching as taught by Darty entails the same functionalities

underlying the above limitation.

As per claim 4, Darty (see Fig. 3c-d) discloses obtaining a second input test vector,

apply it to said sub-module for generating a second output vector; then recursively processing

said submodule and second output test vector would also have been obvious in view of Darty's

above suggestion and the rationale as set forth in claims 1, 3 from above.

As in claim 5, the limitations as to obtaining the submodule and a first input test vector

and apply this to the former would also have been obvious in view of the teachings by Darty in

claim 1 combined with Porterfield because for each repeated step of decomposing sub-routine or

subblock, it will reach a point where a minimal subblock is terminating the decomposition so to

apply a bug list as addressed above in claim 1.

As per claim 6, Darty (combined with Porterfield) discloses appending input test vector

to a test list when the comparison test is positive; repeating the comparison step when the

decompostion test is negative, i.e. when the subblock is minimal; and a first input vector being

reapplied to generate a third output vector (e.g. S153 – Fig 3d; and Fig. 3c); but Darty does not

explicitly teach applying third input in comparison test to recreate the bug; but since the

comparison test is to determine whether a failure still exists in regard to a relevant code block

that previously failed for a known bug, the notion to see recurrence of such bug is disclosed in

Darty steps *S131-S143* – Fig. 3b,c)

As per claim 7, Darty does not disclose two or more subvectors of input test vector but

teaches iteratively processing each input vector to each level of decomposed blocks in a

recursive manner (e.g. S153 – Fig 3d; and Fig. 3c). Thus since Darty has more than one set of

input/outputs and a plurality of dependency sets with which to apply those input vectors (see

steps S104 to S129, Fig. 3a,b); the concept of subvectors from a first input vector being applied

is implicitly disclosed because for each subblocks and dependency subset, some input subset will

be used.

As per claim 8, Darty (combined with Porterfield) discloses iterating through entries of

test/bug list combining more input vectors in association with module name/designation (re

claim 1).

Response to Arguments

4.   Applicant's arguments with respect to claims 1-8 have been considered but are moot in

view of the new ground(s) of rejection.

Conclusion

5.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Tuan A Vu whose telephone number is (272) 272-3735. The

examiner can normally be reached on 8AM-4:30PM/Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Kakali Chaki can be reached on (571)272-3719.

The fax phone number for the organization where this application or proceeding is

assigned is (571) 273-3735 (for non-official correspondence – please consult Examiner before

using) or 703-872-9306 (for official correspondence) or redirected to customer service at 571-

272-3609.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VAT
February 24, 2005

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